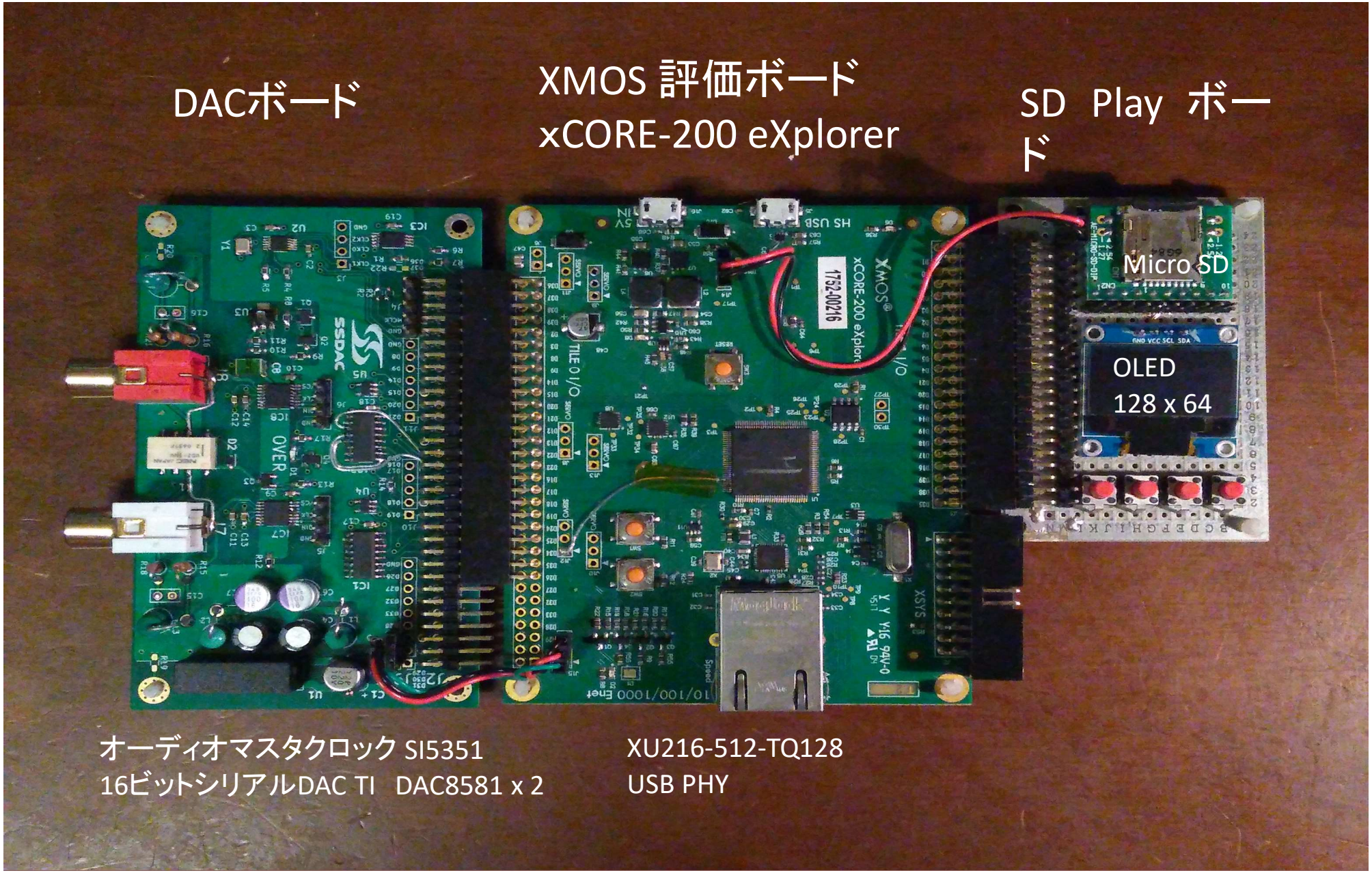
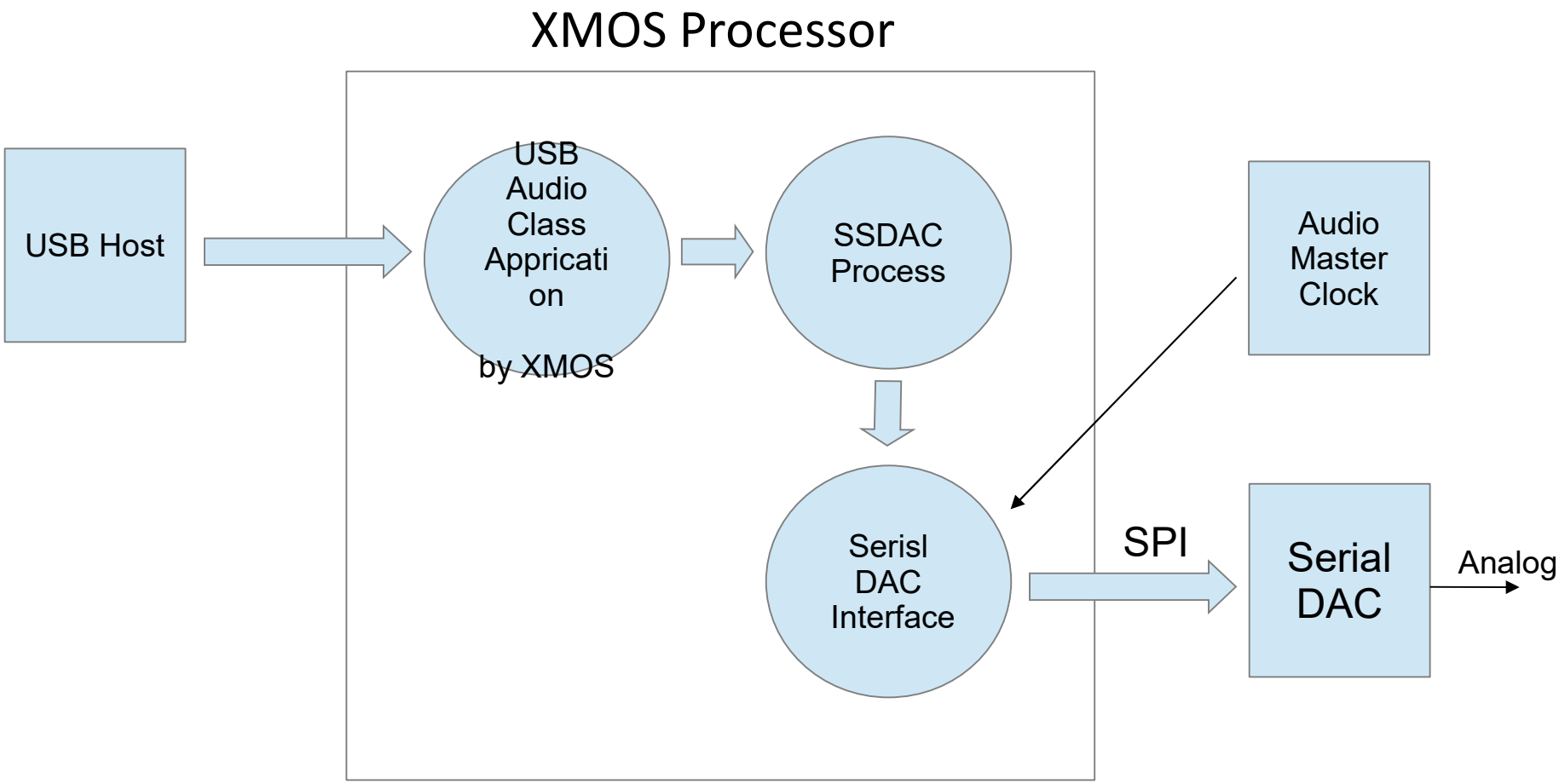
SD CARD PCM Player with SSDAC on XMOS

櫻井@目黒 2020-8-15

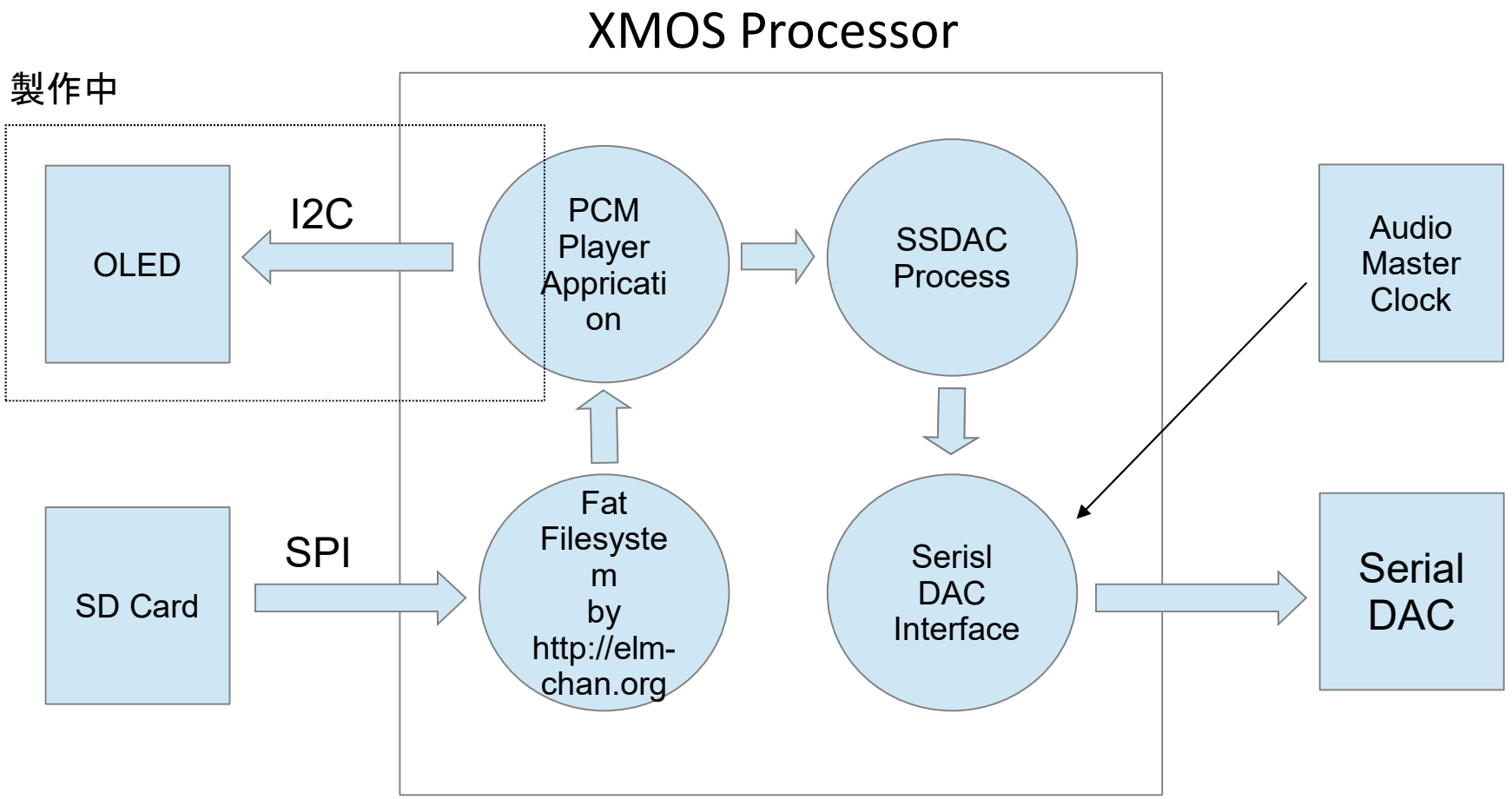


Block Diagram and Software Components (USB Audio)



SSDAC: 32点補間 (@FS = 44.1KHz or 48KHz)

Block Diagram and Software Components (SD Card Player)



http://elm-chan.org

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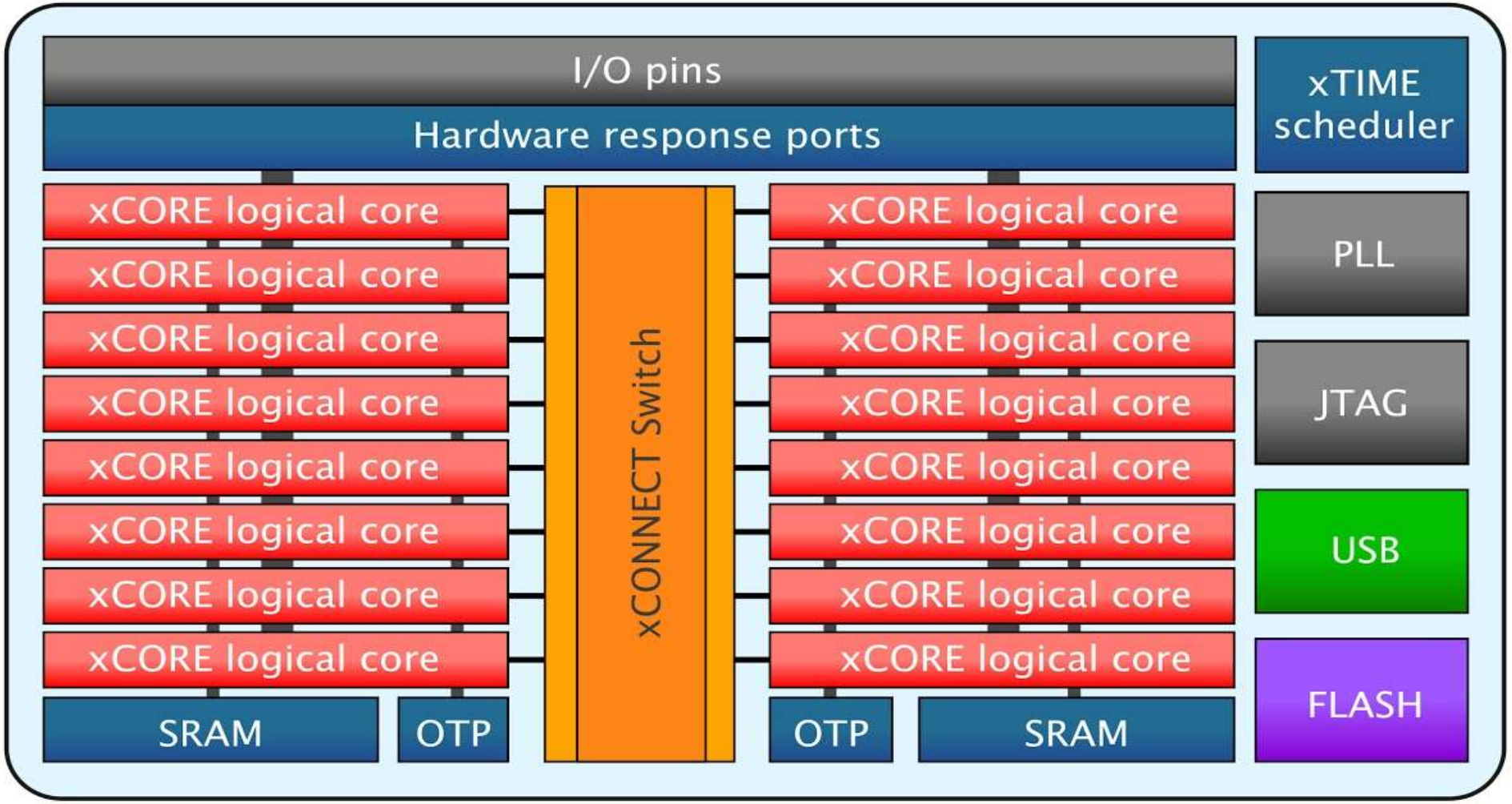
xCORE 200 Archtecture



xCORE-200 XUF216

xCORE Processing Pipline

xTIME™ SCHEDULER

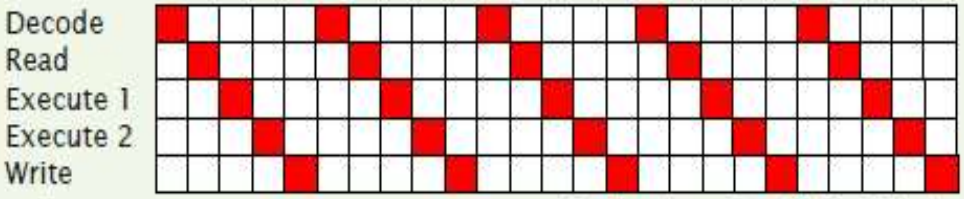
Each xCORE device has one or more tiles. Each tile has up to eight independent 32-bit logical cores that run in parallel without interruption from other cores.

Active cores are guaranteed a minimum level of MIPS. Cores that are idle are not scheduled to the processing resource.

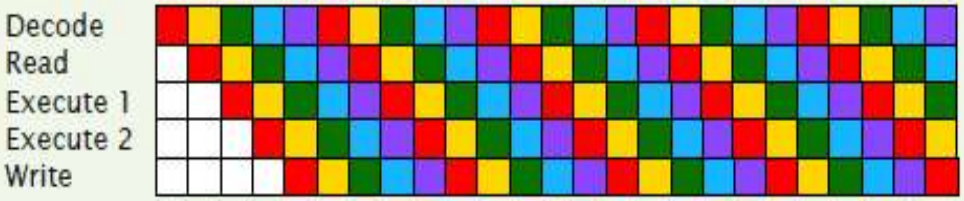
All instructions complete in a single core cycle, or pause the core, waiting for an external event. On xCORE-200 each core can issue up to 2 instructions per clock cycle.

Cores are triggered by events that are managed by the xTIME scheduler. Events that occur at I/O pins are fed directly to a core by the Hardware Response ports. Events can also be generated by timers and tasks, and serviced by the scheduler, with guaranteed behavior.

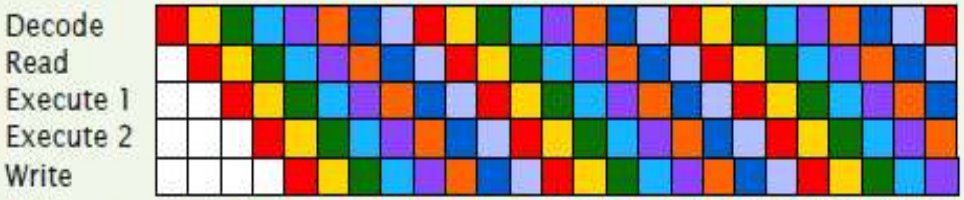
xCORE XL200, XU200, XE200: five stage proecssing pipeline



Single core running: executes every 5 clock ticks (f/5 MHz)



Five cores running: executes every 5 clock ticks (f/5 MHz)



Eight cores running: executes every 8 clock ticks (f/8 MHz)